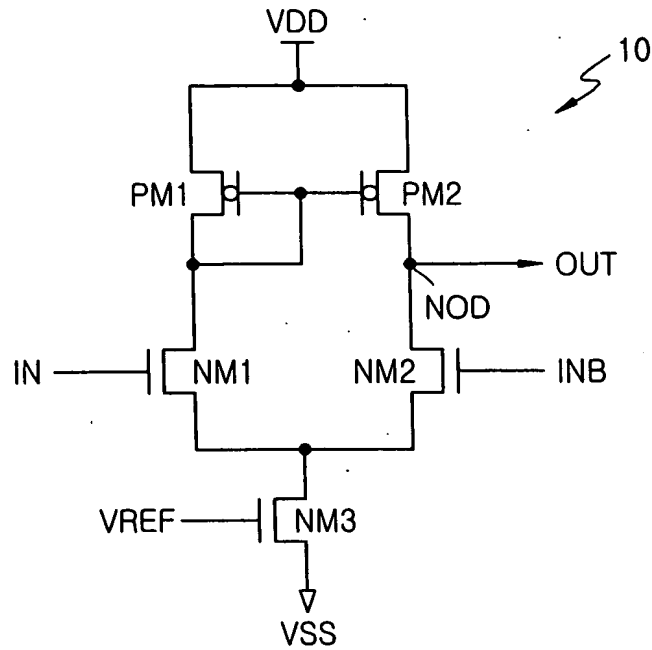


AMPLIFIER CIRCUIT WITH OUTPUT DELAY SELECTIVELY CHANGED ACCORDING TO COMMON
MODE VOLTAGE LEVEL, ASSOCIATED REPLICA DELAY CIRCUIT AND INTERNAL CLOCK
GENERATOR

Application No. NEW - Docket No. SEC.1158

Inventor: Won-ki PARK

FIG. 1 (PRIOR ART)

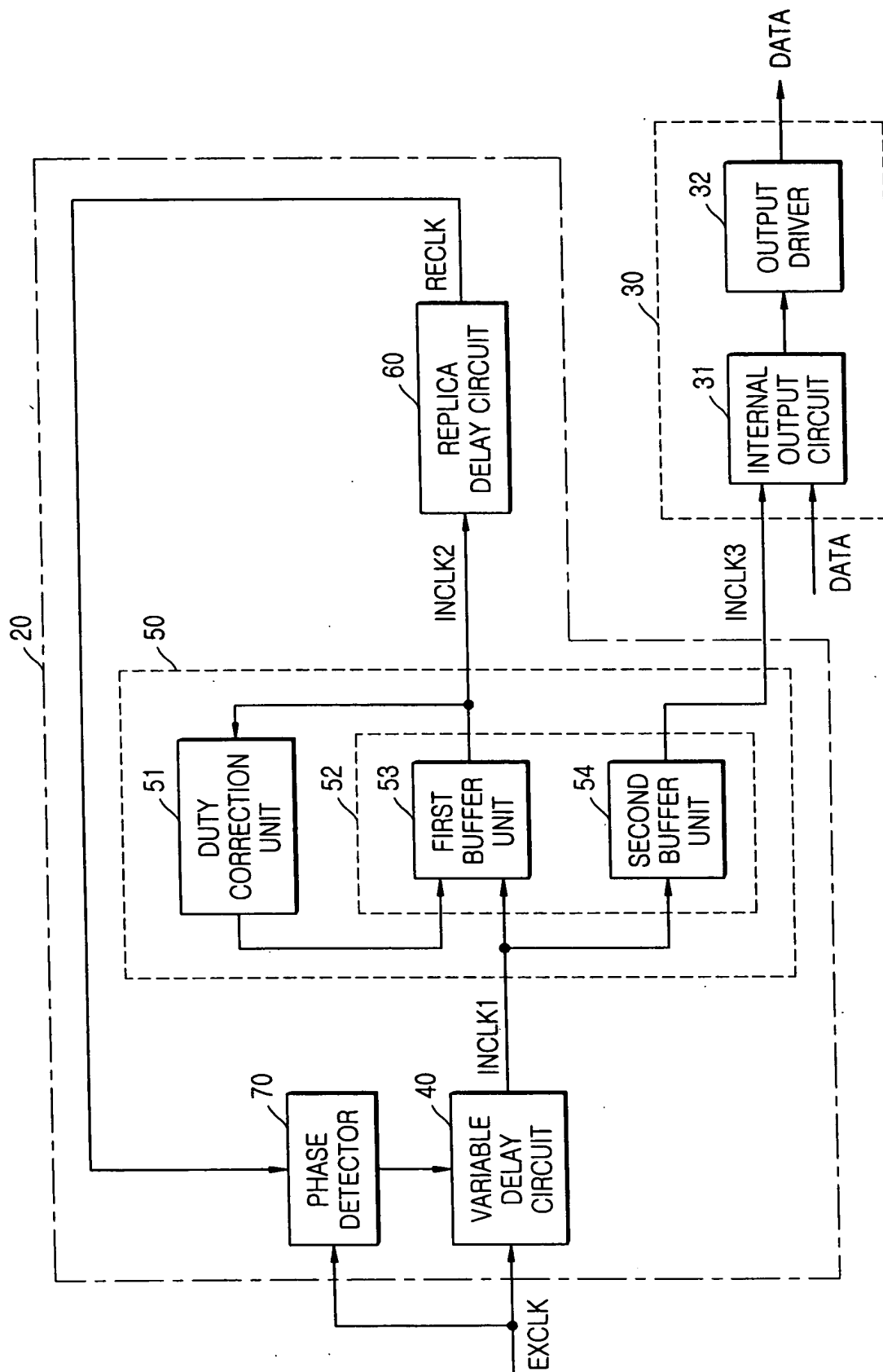


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FIG. 2 (PRIOR ART)



AMPLIFIER CIRCUIT WITH OUTPUT DELAY SELECTIVELY CHANGED ACCORDING TO COMMON
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FIG. 3A (PRIOR ART)

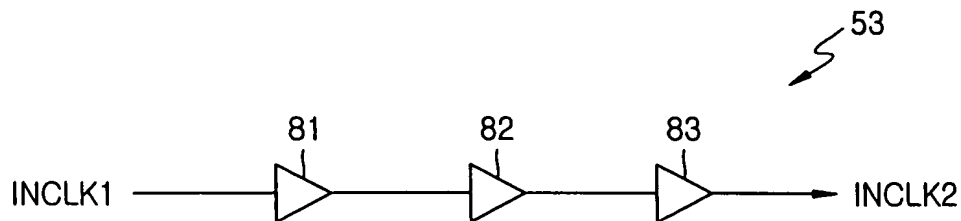
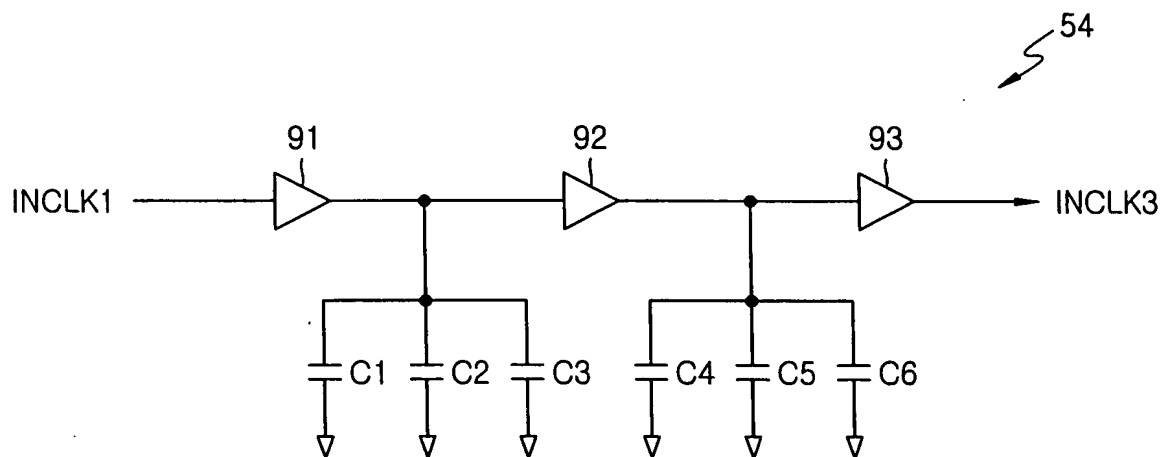


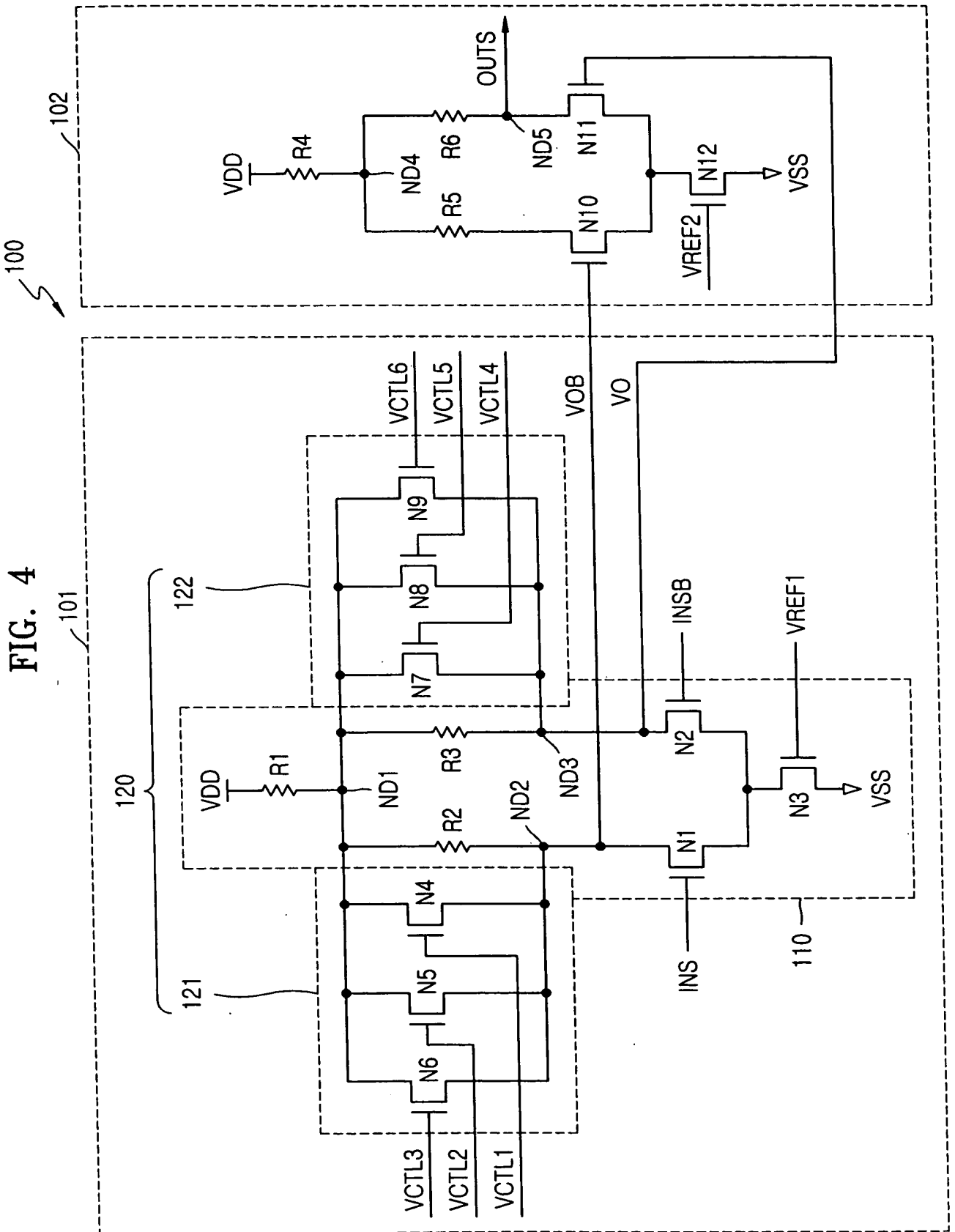
FIG. 3B (PRIOR ART)



AMPLIFIER CIRCUIT WITH OUTPUT DELAY SELECTIVELY CHANGED ACCORDING TO COMMON
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GENERATOR

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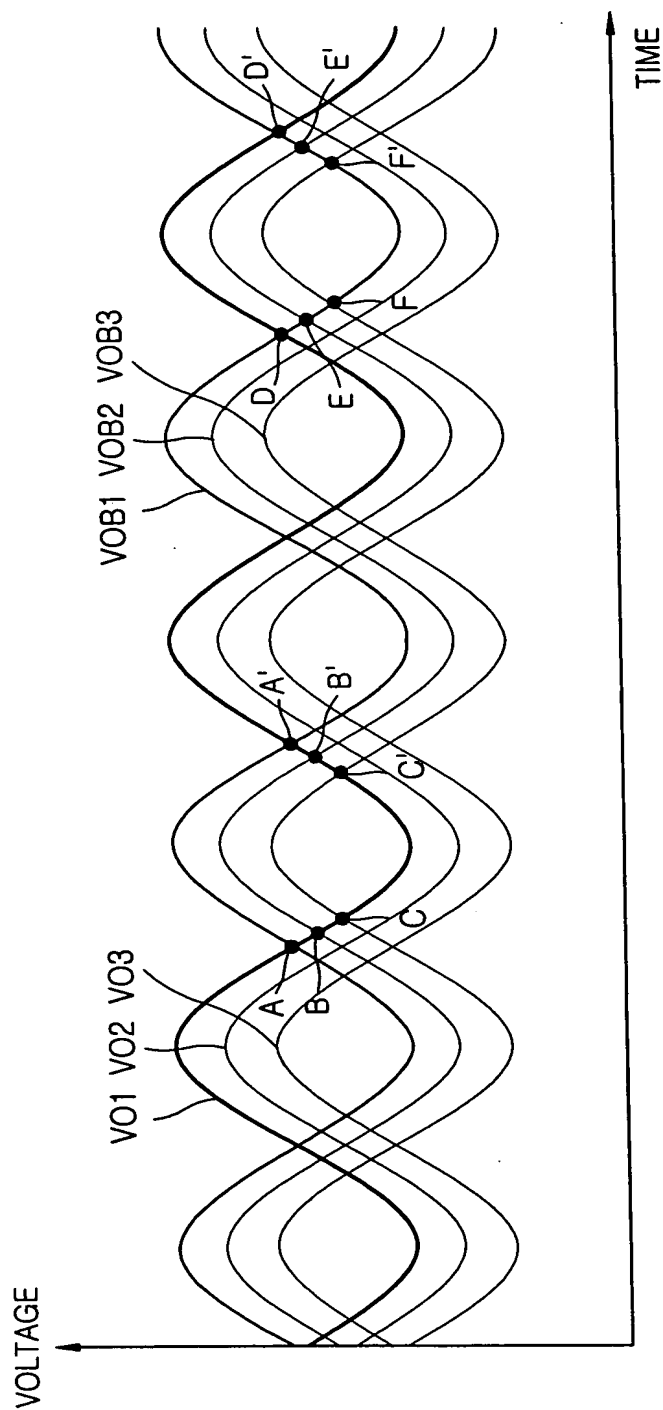


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FIG. 5



AMPLIFIER CIRCUIT WITH OUTPUT DELAY SELECTIVELY CHANGED ACCORDING TO COMMON
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GENERATOR

Application No. NEW - Docket No. SEC.1158

Inventor: Won-ki PARK

FIG. 6A

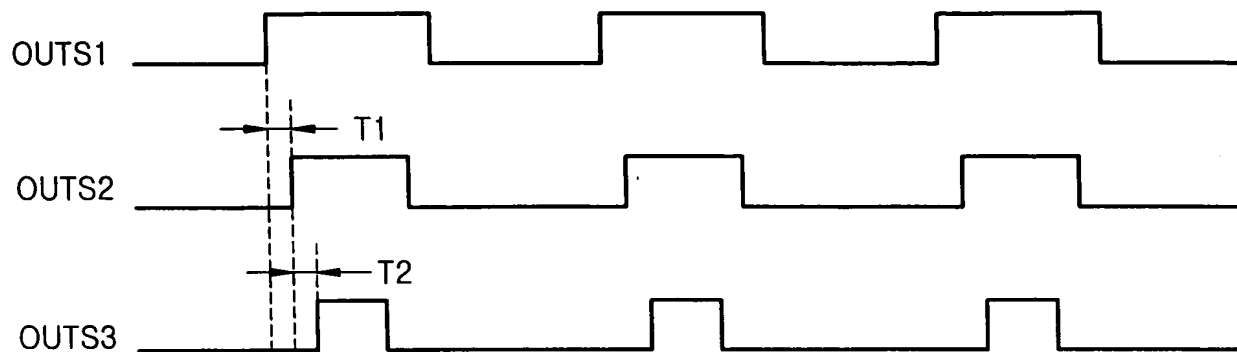
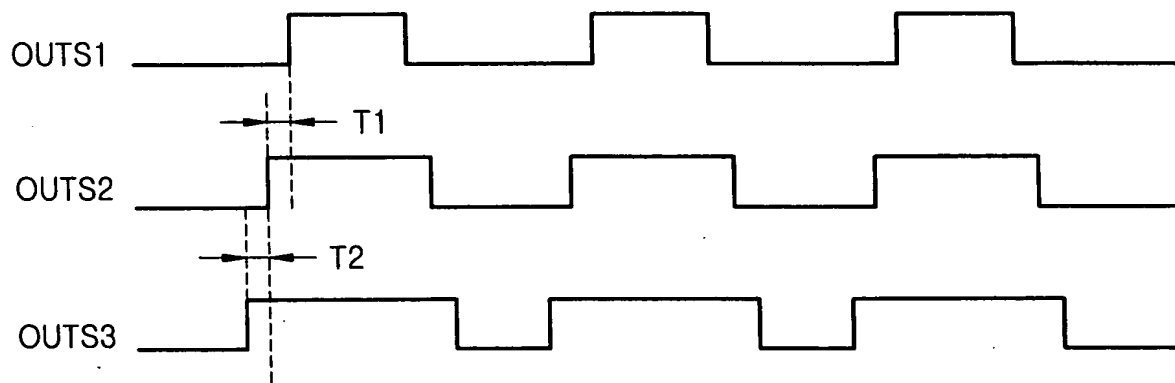


FIG. 6B



Application No. NEW - Docket No. SEC.1158
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The diagram illustrates a PLL circuit 100, which is divided into two main functional blocks: a feedback loop (200) and an output stage (300).

Feedback Loop (200):

- CLK_EX** is the external clock input.
- The **VARIABLE DELAY CIRCUIT (210)** receives **CLK_EX** and outputs **CLK_IN1**.
- The **BUFFER CIRCUIT (220)** receives **CLK_IN1** and outputs **CLK_IN2**.
- The **PHASE DETECTOR (240)** receives **CLK_IN2** and **CLK_RE** (from the replica delay circuit). It outputs a control signal to the **VARIABLE DELAY CIRCUIT (210)**.
- The **REPLICA DELAY CIRCUIT (230)** receives **CLK_IN2** and **VCTL1** (from the control signal generator). It outputs **CLK_RE** to the phase detector.
- The **CONTROL SIGNAL GENERATOR (250)** provides **VCTL1** and **~VCTL6** to the replica delay circuit.

Output Stage (300):

- The **INTERNAL OUTPUT CIRCUIT (301)** receives **CLK_IN2** and outputs **DATA**.
- The **OUTPUT DRIVER (302)** receives **DATA** and outputs the final **DATA** signal.

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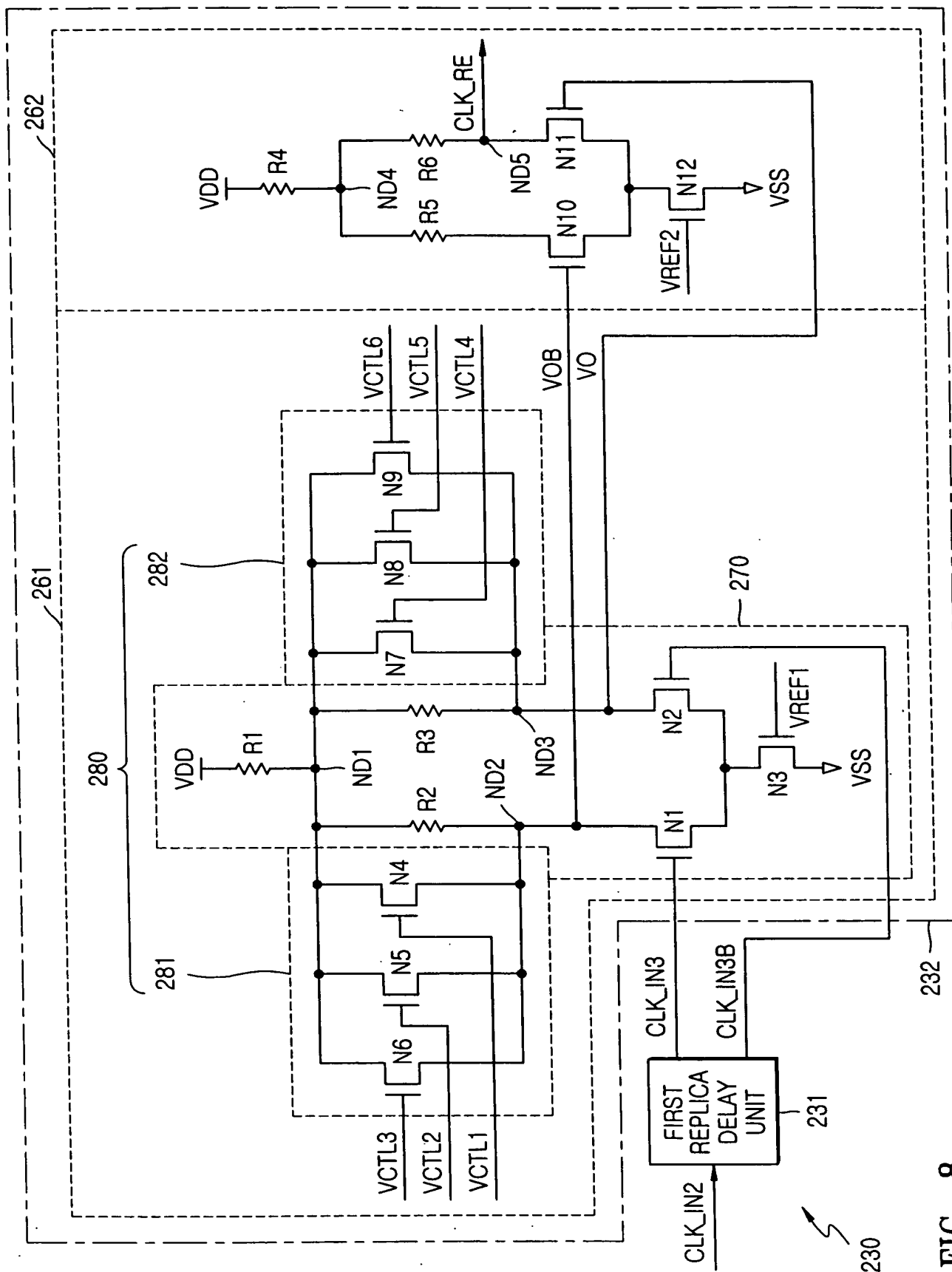


FIG. 8